Digital logic design using VHDL

Class: B.Sc-II

DURATION: ONE YEAR

Mr. S. D. Jadhav

Department of Electronics

1. Title: Digital logic design using VHDL

2. Year of implementation:2020

Structure of Add-on Course

Duration	Theory Hours	Practical Hours	Total Hours	Credits	No. of students in batch
1 Year	10	30	40	02	20

Syllabus

Learning Objectives:

1. To Explain the need of Hardware Description Languages (HDL) to design & Implement digital circuits (combinational & sequential) using VHDL
2. To Develop combinational & sequential logic design skills.

Theory Syllabus (10 Hrs)

Unit I: Introduction to VHDL **(5)**

Introduction to VHDL, Features and Capabilities, entity, architecture with basic gates and derived gates

Unit II: Combinational and sequential logic design **(5)**

Combinational logic design: Half adder, Half substractor, Full adder

sequential logic design: D and RS flip flop, sequential statements, Shift register, Counter

Learning Outcomes:

Upon successful completion of this course, the student will be able to:

1. Describe Features, Capabilities and architecture of VHDL.

2. Describe combinational & sequential logic design skills.

Practical Syllabus (30 Hrs)

Learning Objectives:

1**.** To Factual and Conceptual Knowledge of VHDL Programming

2**.** To Develop HDL codes of digital logic designs

3**.** To Develop combinational logic design using HDLs and verify their performance .

4. To Develop sequential logic design using HDLs and verify their performance .

List of Experiments:----------30hr

1 Study of VHDL Simulator

2 Study of Basic gates

3 Study of Derived gates

4 Study of Half adder

5 Study of Half Substractor

6 Study of Full Adder

7 Study of 4bit full Adder

8 Study of multiplexer

9 Study of Demultiplexer

10. Study of up and down counter

Learning Outcomes:

1. Implement HDL codes of digital logic designs
2. Demonstrate HDL codes of digital logic designs.
3. Demonstrate HDL codes of combinational logic design and verify their performance by synthesis and simulation.
4. Demonstrate HDL codes of sequential logic design and verify their performance by synthesis and simulation.

Recommended Books:

1. Roth, Charles & John Lizy Kurian, Digital Systems Design using VHDL, 2nd Edition, Thomson, 2008 (TK7888.4.R845D 2008)
2. Chu Pong P, RTL Hardware Design using VHDL, John Wiley, 2006 (TK7868.D5C559)
3. Alan B. Marcovitz," Introduction to Logic Design", Third Edition, McGraw Hill
4. Ronald J. Tocci, Neal S. Widmer & Greg Moss, Digital Systems, Global Edition, 12/E,Pearson Education Limited.
5. Bhaskar, A VHDL Primer, Third Edition, Prentice Hall.

BOS Sub Committee:

1. Mr. J. A. Wagh
2. Dr. G. S. Nhivekar
3. Mr. S. K.Shinde
4. Mr. S. R. Pol
5. Mr. S. D. Jadhav
6. Mr .G .R. Attar
7. Mr. S. S. Barkade
8. Mr. P.S. Kadam

Expert Committee:

1. Prin. Dr. B. T. Jadhav
2. Dr. R. K. Kamat
3. Dr. M. K. Bhanarkar
4. Mr. J. A. Wagh